New Approach to GaAs MESFET Analog Frequency Dividers with Low Threshold Input Power and High Conversion Gain

Hicham Amine, Olivier Llopis, Michel Gayral, Jacques Graffeuil, and Jean Francois Sautereau

Abstract—**A new approach to frequency dividers is proposed based on the nonlinear feedback control of MESFET in the forced oscillation mode. The input signal is used to control the MESFET gain, imposing oscillation conditions. A design of frequency dividers based on this approach is proposed and allows the threshold input power to be reduced and the conversion gain to be increased. Frequency division is tested using time domain simulation, and then an *X*-band experimental MESFET analog frequency divider is achieved and exhibits a high conversion gain and a low threshold input power.**

I. Introduction

ANALOG frequency dividers are basic circuits for phase-locked loops and FM communication systems [1]. Many concepts have been put forward to achieve frequency division. Miller's representation [2] is one of the most often used [3]–[6]. Unfortunately, it cannot be used when a single component performs many interactive operations and several electronic functions. Additionally, frequency representations are difficult to use when the circuit is strongly nonlinear and unstable. Other authors have proposed a small signal approach [7] to the design of frequency dividers. Unfortunately some circuit characteristics, like loop gain, depend on the applied signal level and cannot be predicted by these methods.

Our approach is based on the nonlinear feedback control of MESFET in the forced oscillation mode. The input signal is employed to control transistor gain, imposing oscillation conditions. The advantage of this approach primarily lies in the possibility of using a time domain representation which is natural for nonlinear elements. The MESFET is biased near pinch-off. The self-biasing phenomenon relies on the input signal and is responsible for the increase of the MESFET dc transconductance and loop gain at subharmonic frequency.

A simple frequency analysis of MESFET self-biasing phenomenon is performed and its effect on gain is shown. The results obtained are then compared to harmonic balance simulations and to some experimental values. Simulation and measurement allow the threshold input power, and the optimum MESFET gate bias to be determined. Also a technique for reducing the threshold input power is proposed.

Based on the device's self-biasing phenomenon, a frequency divider is presented and analyzed by time domain simulation using ELDO software [8]. Then, an *X*-band $\frac{1}{2}$ frequency divider is simulated and the transmission of FM information is shown. Also, 12 GHz band $\frac{1}{3}$ and $\frac{1}{4}$ frequency dividers have been simulated, demonstrating that this concept can be applied to achieve frequency dividers by any ratio.

By way of example, an experimental MESFET frequency divider (8 GHz → 4 GHz), is achieved and exhibits a high maximum conversion gain ($P_{out}(F_{in}/2)/P_{in}(F_{in})$) (typically 10 dB) and a low threshold input power (−4 dBm).

II. Operation Principle

Fig. 1 shows the block diagram used in our approach for frequency division. The MESFET is the nonlinear element. It is represented by its nonlinear gain $N(e_r)$ as a function of its input er.

When an oscillation occurs the input device voltage can be written as

$$\begin{aligned} Ve_r &= v_{in}(t) + v_{fs}(t) \\ &= V_{in}.\cos(w_{in}.t) + V_{fs}.\cos(w_{fs}.t + \phi). \end{aligned} \quad (1)$$

Using the power series technique [9], it can be shown that the feedback voltage is also given by

$$V_{fs}(t) = \sum_{0}^{\infty} B(p.w_{in} \pm q.w_{fs}) V_{p,q} \cos(p.w_{in} \pm q.w_{fs}).t \quad (2)$$

where $V_{p,q}$ is the voltage value of the $p.w_{in} \pm q.w_{fs}$ pulsation component of the device output.

If a bandpass filter is used as the linear network $B(w)$, a frequency is selected: $r.w_{in} - s.w_{fs}$ which is equal to w_{fs}. Then, the circuit output pulsation is $w_{fs} = r/(s+1)w_{in}$, and the division is performed. This behavior remains consistent as long as the following condition is satisfied:

$$B(r.w_{in} - s.w_{fs}).N(e_r) = 1. \quad (3)$$

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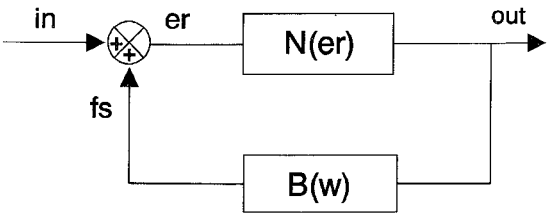

Fig. 1. Black box diagram of frequency divider.

Where $N(e_r)$ is the nonlinear device gain at the subharmonic frequency:

$$N(e_r) = \frac{V_{r,s}}{V_{\text{fs}}}.$$

To avoid free oscillations the following relation must hold irrespective of the frequency:

$$|B(W).N(0)| < 1 \tag{4}$$

The MESFET, biased in the pinch-off region, enables this condition to be verified.

To be able to divide the frequency by 2, the condition (3) becomes

$$\left|N(e_r).B\left(\frac{w_{\text{in}}}{2}\right)\right| > 1$$

$$\text{Arg}\left\{N(e_r).B\left(\frac{w_{\text{in}}}{2}\right)\right\} = 2.\text{k}.\pi \qquad k \text{ integer}$$

The first condition is obtained by increasing the MESFET gain thanks to the self-biasing of its drain current by the input signal. The second condition requires adjusting the phase in the loop.

The advantage of this approach lies in the possibility of obtaining frequency division by any ratio using one nonlinear element. This element (the MESFET) is biased near pinch-off to increase the nonlinearity order. Moreover, such a general approach can be used with any type of nonlinear device; only the self-biasing gain dependence is needed.

III. Analysis and Simulation

A. Device Modeling

The MESFET model [10] employed for simulation is shown in Fig. 2. The linear parameters of the model are deduced from the measured S parameters for different frequency values. A simplified model is established using drain current generator as the only nonlinear element. This drain current is the most significant element in the model and is described by TAJIMA expressions [10]. Parameter values for these expressions are derived from pulsed measurements to prevent any trapping problems [12]. In order to restrain any thermal variation of the drain current, self-biasing must not be too high. However, simplified modeling becomes insufficient for high input power level and to achieve a more accurate model, other nonlinearities must be taken into account like the gate diode current to limit the gate voltage excursion and the gate capacitance nonlinearity which depends on the input power level.

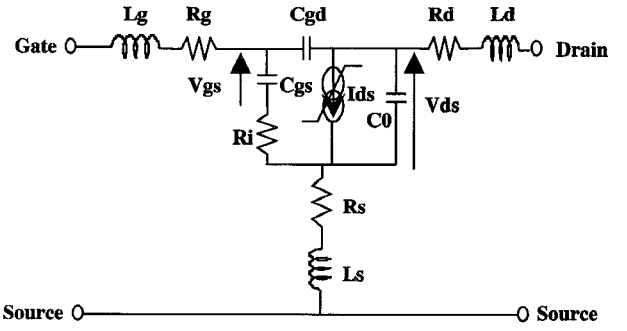

Fig. 2. Nonlinear MESFET model.

Taking into account the element values of the equivalent circuit of Fig. 2, some of these elements (Ls, Rs and Cgd) can be deleted to do an approached frequency domain analysis. The drain current is approximated by

$$Ids(t) = Ids[Vgs(t), Vds(t)] = Ids(Vgs) + \frac{\partial Ids}{\partial Vds}.Vds$$

Where

$$Ids(Vgs) = Idss\left(1 - \frac{Vgs}{Vt}\right)^2 \qquad \text{if } Vgs > Vt$$

$$Ids = 0 \qquad \text{if } Vgs < Vt \tag{5}$$

$\partial Ids/\partial Vds = 1/R0$ is represented by a linear resistor, $Idss$ is the drain saturation current and Vt the pinch-off voltage value.

B. Frequency Domain Analysis

This analysis is based on Fourier Transform. It permits understanding of the self-biasing phenomenon. This technique is relatively easy to use but requires a simplified assumption (5) on the MESFET nonlinearity. The MESFET input signal may be written as

$$V_{er} = V_{\text{in}}.\sin(2.\pi.F.t) + V_{\text{fs}}.\sin\left(2.\pi.\frac{F}{2}.t + \varnothing\right)$$

Where V_{fs} is a small signal representing the beginning of an oscillation at $F/2$ frequency, $F = F_{\text{in}}$ and V_{in} the input signal, with

$$V_{\text{fs}} \ll V_{\text{in}} \tag{6}$$

The gate signal is given by:

$$Vgs = V_{gs1}.\cos(2.\pi.F.t + \psi_2) + V_{gs2}.\cos.\left(2.\pi\frac{F}{2}t + \psi_1\right) + V_{gso} \tag{7}$$

The MESFET is biased near pinch-off. Then

$$V_{gso} - Vt \ll Vt \tag{8}$$

The MESFET drain current is calculated using (5) and

(7):

$$Ids(t) = \sum_{0}^{\infty} Ids_n . \cos\left(n.2.\pi . \frac{F}{2} t + \varphi_n\right)$$

$$Ids_n = \frac{2}{T}\int_0^T Ids(t) . \cos\left(n.2.\pi . \frac{F}{2} t\right) dt \qquad \text{for } n > 1 \tag{9}$$

The dc drain current Ids_o and the transconductance gm_o are given respectively by

$$Ids_o = \frac{1}{T}\int_0^T Ids(t)\, dt \cong \frac{Idss}{4} . \frac{V_{gs1}^2}{Vt^2} + Idss\left(1 - \frac{V_{gso}}{Vt}\right)^2$$

$$gm_o = \frac{1}{T}\int_0^T \frac{\partial Ids}{\partial Vgs}\, dt \cong \frac{Idss}{\pi} . \frac{V_{gs1}}{Vt^2} - 2 . \frac{Idss}{Vt} \tag{10}$$

$$\cdot \left(1 - \frac{V_{gso}}{Vt}\right). \tag{11}$$

Equations (10) and (11) show that Ids_o (Fig. 3) and gm_o increase with the input value V_{in}. The MESFET gain increases according to the transconductance value. The MESFET power gain is calculated using (9) and taking into account the simplified assumptions (6) and (8) as

$$|N(e_r)| \cong \left(\frac{Idss}{Vt^2}\right)^2 \left|\left\{\frac{V_{in}}{4.K1} + 2 . (V_{gso} - Vt)\right\}^2 . \frac{4.Zc.Ze}{K2^2}\right|, \tag{12}$$

where Zc is the input loading impedance. It is assumed to be real ($Zc = 50$)

$$K1 = \sqrt{1 + (2.\pi.Ci(Ri + Zc + Rg)F)^2},$$

$$K2 = \sqrt{1 + (\pi.Ci(Ri + Zc + Rg)F)^2},$$

$$Ze = \mathrm{Re}(Z_{out}) \left|\frac{Z_{ds}}{Z_{out} + Z_{ds}}\right|^2,$$

Z_{out} is the output loading impedance and Z_{ds} is the drain impedance.

MESFET gain increases with the input power according to relation (12). This gain also increases with the gate bias voltage, and to avoid spontaneous free oscillation, condition (4) leads to

$$|N(0)| = 4\left(\frac{Idss}{Vt^2}\right)^2 \left|\frac{4.Zc.Ze.(V_{gso} - Vt)^2}{K2^2}\right| < \frac{1}{B(w)}. \tag{13}$$

The threshold input voltage V_{th} can be calculated using

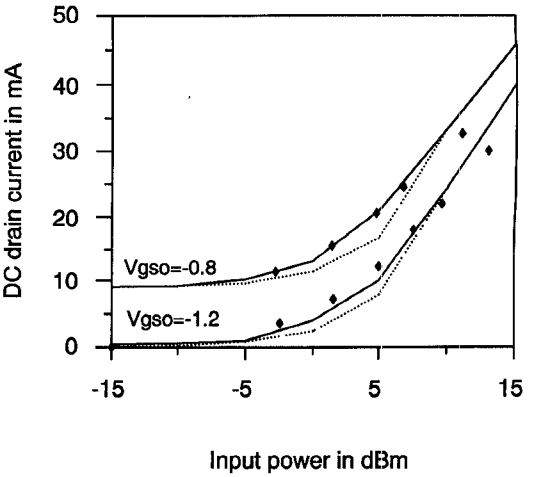

Fig. 3. Simulated (solid line), analytic (dashed line) and measured (♦) MESFET dc drain current versus the input power.

(12) as

$$V_{th} \cong 4.K1\left\{\frac{Vt^2.K2}{2.Idss.\sqrt{|Ze.Zc.B(w)|}} - 2.(V_{gso} - Vt)\right\}. \tag{14}$$

To reduce the threshold input power the gate bias voltage must be as high as possible. However (13) must always be satisfied. Then the maximum gate bias voltage is:

$$V_{gso|} = Vt\left\{1 + \frac{Vt.K2}{2.\sqrt{|B(w).Ze.Zc|}.Idss}\right\}. \tag{15}$$

Therefore, the MESFET must exhibit a high drain saturation current $Idss$ value and a low pinch-off voltage Vt to maximize the MESFET gain value.

This technique allows the threshold input power to be determined but cannot be used to analyze the steady state. Assumption (6) becomes invalid in steady state and an analytical solution to Fourier integral cannot be obtained. Furthermore, the MESFET will not work as a classical mixer because the RF signal (V_{fs}) is a large signal. As a result, the harmonic balance simulation and time domain simulation were used to overcome this problem.

C. Simulation

The frequency domain technique is easy to perform but insufficient for high input power ($P_{in} > 6$ dBm). The quadratic approximation of the drain current of the MESFET cannot be applied. Furthermore the simplified relations for the drain current (10) and MESFET gain value (12) are not valid when the dc gate is not biased in the pinch-off zone. Accurate simulation in open loop configuration is performed using the harmonic balance simulator LIMHA software from the University of Limoges [11]. In this simulation a severe MESFET model and strict drain relations [10] are used.

The dc drain current (Fig. 3) and open loop MESFET gain $N(e_r)$ for the $F/2$ oscillation (Fig. 4) are simulated

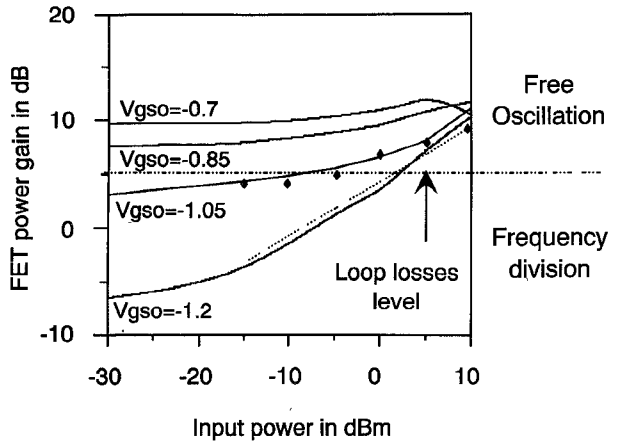

Fig. 4. Simulated (solid line), analytic (dashed line) and measured (♦) MESFET nonlinear gain of subharmonic component (F_{fs} = 4 GHz, P_{fs} = −20 dBm) in open loop configuration versus the input power (F_{in} = 8 GHz).

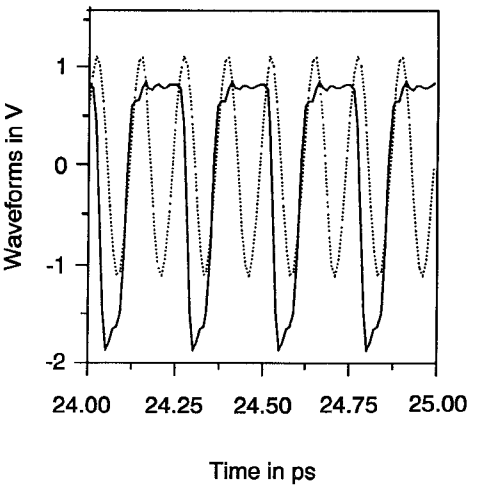

Fig. 5. Simulated output waveform (solid line) of $\frac{1}{2}$ frequency divider.

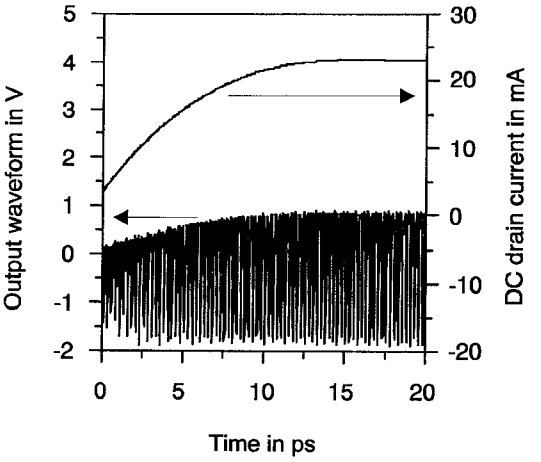

Fig. 6. Simulated MESFET dc drain current and output $\frac{1}{2}$ frequency divider waveforms.

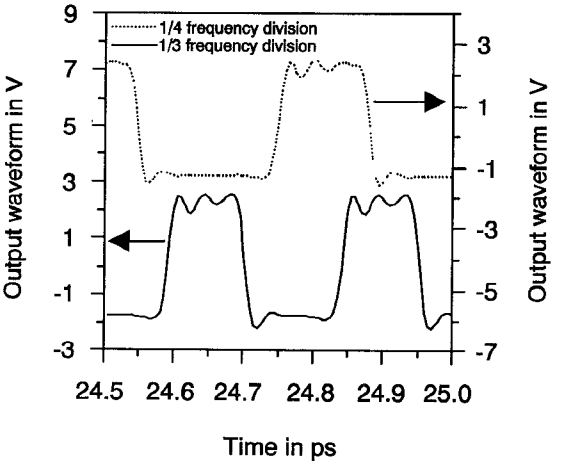

Fig. 7. Simulated $\frac{1}{3}$ and $\frac{1}{4}$ frequency dividers output waveforms for a sinusoidal input signal (F_{in} = 12 GHz, P_{in} = 5 dBm)

as a function of the input power for different dc gate bias values. Then, a good agreement is found between analytic and simulated results. The gain increases with the input power and dc gate bias voltage. When a $F/2$ frequency oscillation occurs in the circuit, it can be maintained when the MESFET gain $N(e_r)$ value is higher than the loop losses.

Fig. 4 shows the frequency division region and the free running oscillation region when the loop losses are about 5 dB. Note that to avoid spontaneous free oscillations, the gate bias voltage V_{gso} must be less than −1.0 V. Thus the optimum value of V_{gso} is −1.0 V. Also worthy of note is the good agreement between the theoretical results (harmonic balance and frequency domain analysis) and experimental ones.

The harmonic balance simulations are efficient in determining the open loop characteristics of the circuit but cannot be used for the analysis of the frequency division range or to predict the output power value in steady state. We therefore performed a time domain simulation [13] of the frequency division using the ELDO software. The input and output waveforms for the $\frac{1}{2}$ frequency divider (F_{in} = 8 GHz, F_{out} = 4 GHz) are shown in Fig. 5. To reduce the threshold input power the gate bias voltage (V_{gso} = −1 V) is predicted from the simulated gain (Fig. 4). The $F/2$ component of the output wave is calculated using a FFT program.

The self-biasing phenomenon is observed by simulation. Fig. 6 shows the dc drain current simulated from the beginning of the $F/2$ oscillation to steady state. It goes from one value, imposed by external dc bias voltage (3 mA), to a higher value (22 mA) enabling oscillation to continue.

As an example of other division ratio simulation, Fig. 7 shows the output waveform of $\frac{1}{3}$ and $\frac{1}{4}$ frequency dividers simulated for a sinusoidal input signal (F_{in} = 12 GHz, P_{in} = 5 dBm).

The transmission of the informative signal is also verified by frequency modulation of the input signal. Thus, it can be assumed that

$$v_{in}(t) = V_{in}.\cos\left[2\pi.F.t + m_{in}\cos\left(2\pi.F_{m1}.t\right)\right]$$

where

$$m_{in} = 1 \text{ and } F_{m1} = 3 \text{ MHz}$$

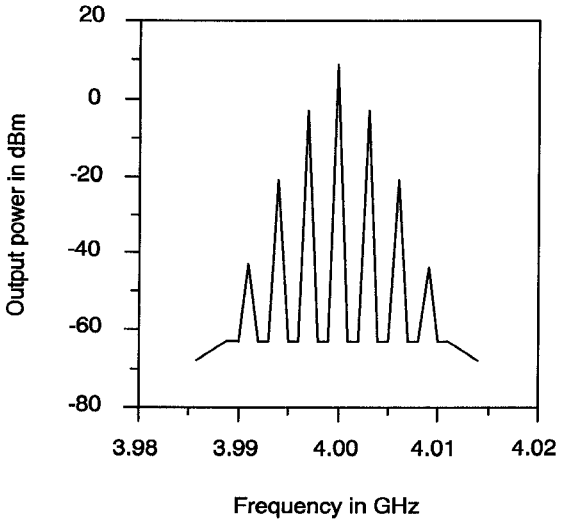

Fig. 8. Simulated output spectrum for a frequency modulated input signal (P_{in} = 0 dBm, m_{in} = 1, F_{in} = 8 GHz, F_{m1} = 3 MHz).

The output waveform is simulated and its spectrum (Fig. 8) is calculated using a FFT program. The simulation output can be assumed as the frequency modulated signal:

$$v_{out}(t) = V_{out}.\cos\left[2\pi.\frac{F}{2}.t + m_{out}.\cos(2\pi.F_{m2}.t)\right]$$

with

$$m_{out} = 0.48 \cong \frac{m_{in}}{2} \text{ and } F_m = F_{m2} = F_{m1} = 3 \text{ MHz}.$$

The present divider can therefore be used for FM communication or PLL circuits.

IV. Experimental Results

The dc drain current is measured in open loop configuration. This current increases with the input power as shown in Fig. 3. This is consistent with the simulation of Section (III-B) and the theoretical relation (10). Therefore, it allows the self-biasing to be validated. Moreover, the measured MESFET open loop gain (Fig. 4) increases as predicted by the simulation and the theoretical analysis.

The measured, theoretical and simulated values of the dc drain current and the MESFET gain are compared and turned out to be in good agreement. This enables the nonlinear modeling of the MESFET to be validated.

Based on self-biasing, an experimental frequency divider by 2 has been achieved and its block diagram is represented in Fig. 9. The combiner is a circulator, the phase shifter is produced by a variable length transmission line and the feedback obtained by a 3 dB power divider.

The MESFET is a MGF1412. DC bias is derived from simulation (V_{gso} = −1.0 V and V_{dso} = 3 V). The measured dc drain current varies from a low value (0.05 *Idss* for P_{in} = 0 mW to a high value (0.4 *Idss*) for P_{in} = 10 mW and thus shows the influence of the self-biasing during frequency division. The output power and dc drain current are measured for different gate bias values as given in Fig. 10. The optimum dc gate bias is −1 V, the threshold input power is −4 dBm, the maximum conversion gain 10 dB, and the present divider could operate on the (−5.0, +10 dBm) input power range with a conversion gain higher than 2 dB. Note that the experimental and theoretical values of the optimum dc gate bias, the conversion gain and the threshold input power are in good agreement.

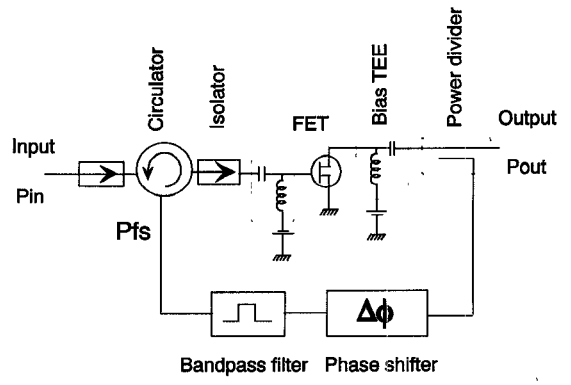

Fig. 9. Schematic of the experimental analog frequency divider.

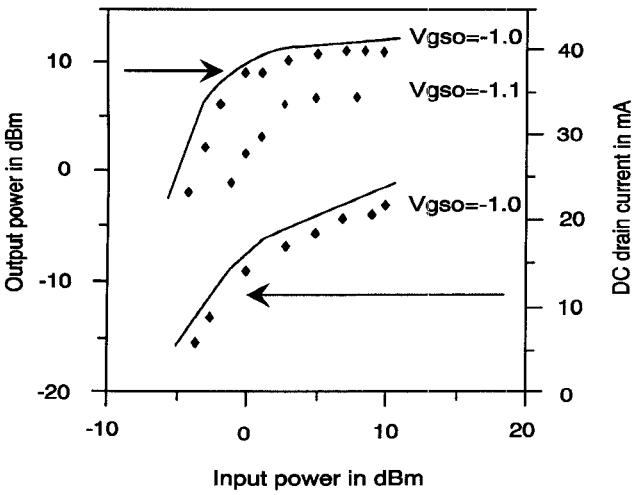

Fig. 10. Frequency divider output power (F_{out} = 4 GHz) and MESFET dc drain current versus the input power (F_{in} = 8 GHz): measurement (♦) and simulation (solid line).

The transmission of a FM informative signal is verified for different modulation frequencies and power levels. Fig. 11 shows the measured spectrum of the frequency divider output when the input signal is frequency modulated with: F_{m1} = 3 MHz, m_{in} = 1, P_{in} = 0.0 dBm and F_{in} = 8.015 GHz. The measured output is frequency modulated with: F_{m2} = 3 MHz, m_{out} = 0.5, P_{out} = 8.7 dBm and F_{out} = 4.007 GHz. This is consistent with the simulated results described in Section (III-B).

Finally, the performance of such a circuit is better than classical MESFET frequency dividers. The conversion gain of these circuits are currently less than 0 dB and their thresholds input power are higher than 0 dBm.

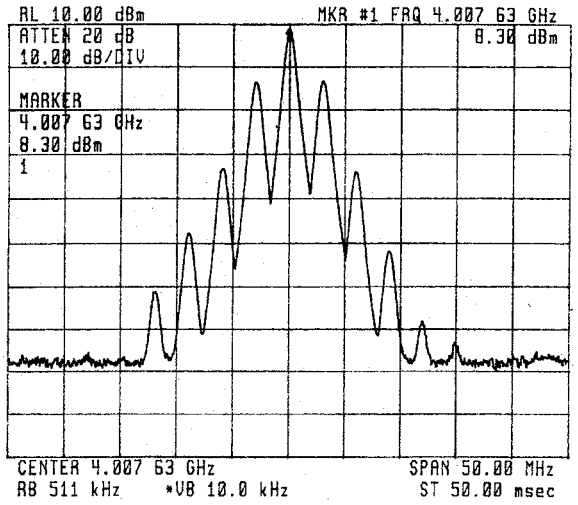

Fig. 11. Measured output spectrum of the frequency divider for a FM input signal with F_{in} = 8.007 GHz, F_{m1} = 3 MHz, P_{in} = 0 dBm, m_{in} = 1.

Conclusion

An original concept of frequency dividers based on the self-biasing phenomenon has been proposed. This concept has been validated by frequency domain analysis and harmonic balance simulations. This allows $\frac{1}{2}$, $\frac{1}{3}$ and $\frac{1}{4}$ frequency dividers to be simulated using a time domain analysis. Then an experimental frequency divider has been produced, exhibiting a high conversion gain and a low threshold input power. Additionally the transmission of a frequency modulation has been checked and showed that these frequency dividers can be used in FM transmission and PLL systems.

The good agreement between simulated and experimental results confirms our model and technique. Moreover, it has been shown that drain current nonlinearity is sufficient to describe MESFET behavior in frequency dividers.

Finally, this proposed approach can be applied to other devices to perform frequency division by any ratio.

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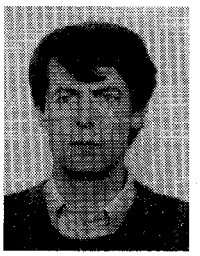

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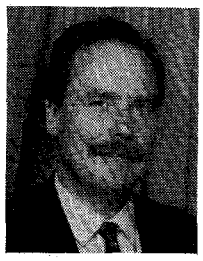

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Since 1972, he has been an Assistant Professor at Paul Sabatier University. At the same time, he joined the Laboratoire d'Automatique et d'Analyse des Systèmes du Centre National de la Recherche Scientifique (LAAS-CNRS), Toulouse, where he was engaged in research on noise in semiconductor devices and circuits. His first area of interest was Gunn oscillators. Since 1974 he has been involved with the study of GaAs MESFET. He is currently Professor of Electronical Engineering at Paul Sabatier University, Toulouse, France and the Director of the whole Paul Sabatier University continuous education service. His current activities are in the area of MESFET's, HEMT's, HBT's, noise and nonlinear properties of these devices and related circuits. Special attention is given to MMIC design. Pr SAUTERAU has authored or co-authored over 87 technical papers and five books.